Q.P. Code: 19EC4209 **R19**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year II Semester Regular Examinations October-2020

FPGA ARCHITECTURES & APPLICATIONS

(VLSI)

TIme: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Draw the structure of PAL and explain it.	**6M**
	b	Discuss about speed performance and in-system programmability of lattice PLST's architecture in 3000 series.	**6M**

OR

2	**a**	Compare the salient features of AMD's CPLD Mach 1 to 5.	**6M**
	b	Draw the structure of PLA and explain it.	**6M**

UNIT-II

3	**a**	Write about FPGA and compare the speed performance of ACT1, ACT2, and ACT3 FPGA.	**6M**
	b	Give the basic properties of petrinet Explain the traffic light controller design using Petrinet notation.	**6M**

OR

4	**a**	Explain the functions of different blocks in Xilinx XC4000 CLB.	**6M**
	b	Explain the design flow of FPGAs.	**6M**

UNIT-III

5	**a**	Discuss the problem of initial state assignment for one hot encoding and explain the procedure to design a state machine.	**6M**
	b	Write about linked state machine.	**6M**

OR

6	**a**	Explain the procedure for design a state machine using one hot encoding.	**6M**
	b	Explain about symbolic representation of FSM architectures and how it is different from ASM.	**6M**

UNIT-IV

7	**a**	Design a data path bus using one –hot method.	**6M**
	b	Explain about the top down design approaches of a state machine.	**6M**

OR

8	**a**	Explain K application of one –hot method.	**6M**
	b	State machine design centered around shift registers.	**6M**

UNIT-V

9	**a**	Explain the Combinational Logic circuits.	**6M**
	b	Design a BCD counter using appropriate programmable logic elements or device.	**6M**

OR

10	**a**	Explain about Decade counters.	**6M**
	b	Design a 4-bit parallel adder circuit.	**6M**

*** END ***